16   a thread identification pipeline in parallel with

17   the instruction decode pipeline and the valid bit

18   pipeline, the thread identification pipeline having the

19   same predetermined number of pipe stages in parallel

20   with the predetermined number of pipe stages of the

21   instruction decode pipeline and the valid bit pipeline,

22   the thread identification pipeline to associate a

23   thread identification at each pipe stage with each

24   instruction being decoded in the instruction decode

25   pipeline.

1   38. (New)   The pipelined instruction decoder of

2   claim 37 further comprising:

3   a pipeline controller coupled to the

4   instruction decode pipeline, the valid bit

5   pipeline, and the thread identification pipeline,

6   the pipeline controller to separately control the

7   clocking of each pipe stage of the instruction

8   decode pipeline, the valid bit pipeline, and the

9   thread identification pipeline.

1   39. (New)   The pipelined instruction decoder of

2   claim 38 wherein

3   the pipeline controller includes clear logic

4   for each pipe stage, the clear logic to control

5   the invalidation of instructions in each pipe

6   stage of the instruction decode pipeline by

7	setting a valid bit in a respective pipe stage of
8	the valid bit pipeline to indicate an invalid
9	instruction.

1	40. (New) The pipelined instruction decoder of
2	claim 38 wherein
3	the pipeline controller includes
4	powerdown logic to analyze the valid
5	indicator of each pipe stage to determine if a
6	next pipe stage is to be powerdowned and to
7	determine if a pipe stage is to be stalled; and
8	clock control logic to determine if
9	respective clock signals to a pipe stage of the
10	instruction decode pipeline, the valid bit
11	pipeline, and the thread identification pipeline
12	are to be stopped to conserve power or preserve
13	data during a stall.

1	41. (New) The pipelined instruction decoder of
2	claim 38 wherein
3	the powerdown logic of the pipeline controller to
4	analyze the valid bit of each pipestage to determine if any
5	pipestage should be stalled,
6	the powerdown logic including
7	an exclusive-OR (XOR) gate to exclusively OR
8	a thread identification of a next to last pipe

9   stage with a thread identification of a stall to

10   determined if they match, and

11   a first AND gate to AND a valid bit of the

12   next to last pipe stage with an output of the XOR

13   gate,

14   in order to determine if a pipe stage prior

15   to the next to last pipe stage should be stalled.

1   42. (New)   The pipelined instruction decoder of

2   claim 41 wherein

3   the powerdown logic further including,

4   a second AND gate to AND the valid indicator

5   of the pipe stage for which the determination is

6   being made with the valid indicator of the next

7   pipe stage, and

8   a third AND gate to AND an output of the

9   second AND gate with an output from the first AND

10   gate,

11   in order to determine if a pipe stage other

12   than the next to last pipe stage should be

13   stalled.